AMENDMENTS TO THE CLAIMS:

Claim 1 (currently amended): A signal switching apparatus comprising:

a plurality of buses~~, each of said buses assigned a number~~;

a first ~~checking signal generating~~ oscillator device that generates first checking signals used for checking ~~a left channel~~ an output path and is capable of providing the generated first checking signals to at least a first group of the plurality of buses;

a second ~~checking signal generating~~ oscillator device that generates second checking signals used for checking ~~a right channel~~ an output path and is capable of providing the generated second checking signals to only a second group of the plurality of buses, the first checking signals and the second checking signals different from each other; and

a checking signal input device that ~~causes the first checking signals to be input to buses based on their respective odd numbered assignment and~~ causes the second checking signals to be input to ~~buses based on their respective even numbered assignment~~ the second group of the plurality of buses and causes the first checking signals to be input to the first group of the plurality of buses.

Claim 2 (currently amended): A signal switching apparatus ~~according to claim 1, further~~ comprising:

a plurality of buses;

a first oscillator device that generates first checking signals used for checking an output path and is capable of providing the generated first checking signals to one or more buses from the plurality of buses;

a second oscillator device that generates second checking signals used for checking an output path and is capable of providing the generated second checking signals to only a group of buses from the plurality of buses, wherein the first checking signals and the second checking signals are different from each other;

a selecting device that selects both the first checking signals and the second checking signals or only the first checking signals as checking signals to be input to all of said plurality of buses, and

a checking signal input device that ~~controlling device that controls said checking signal input device so as to cause~~ causes the second checking signals to be input to the group of buses and the first checking signals to be input to the other buses of the plurality of buses ~~the buses assigned respectively odd numbers and the second checking signals to be input to the buses assigned respectively even numbers~~ if said selecting device selects both the first checking signals and the second checking signals, and ~~cause~~ causes the first checking signals to be input to all of said plurality of buses if said selecting device selects only the first checking signals.

Claims 3-5 (canceled)

Claim 6 (new): A signal switching apparatus according to claim 1,

wherein the first group of the plurality of buses includes two or more buses,

wherein the second group of the plurality of buses includes two or more buses,

wherein the plurality of buses consists of the first group of the plurality of buses and the second group of the plurality of buses, and

wherein the second group of the plurality of buses does not include any of the first group of the plurality of buses.

Claim 7 (new): A signal switching apparatus according to claim 1,

wherein the first checking signals and the second checking signals represent a sine waveform.

Claim 8 (new): A signal switching apparatus according to claim 2,

wherein the first checking signals and the second checking signals represent a sine waveform.